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PATENT APPLICATION

ATTORNEY DOCKET NO. 200302181-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): James Reuter	Confirmation No.: 4878
Application No.: 09/872,962	Examiner: Nawaz, Asad M.
Filing Date: June 1, 2001	Group Art Unit: 2152

Title: CENTRALIZED FINE-GRAINED ENHANCEMENTS FOR DISTRIBUTED TABLE DRIVEN I/O MAPPING

Mail Stop Appeal Brief - Patents
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TRANSMITTAL OF REPLY BRIEF

Transmitted herewith is the Reply Brief with respect to the Examiner's Answer mailed on January 26, 2007 .

This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new ground rejection.)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
James Reuter	)	Group Art Unit: 2152
	)	
Serial No.: 09/872,962	)	Examiner: Nawaz, Asad M.
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For: CENTRALIZED FINE-GRAINED ENHANCEMENTS FOR DISTRIBUTED TABLE DRIVEN I/O MAPPING

REPLY BRIEF

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed January 26, 2007.

ARGUMENT

I. Rejections Under 35 U.S.C. §102

Claims 1-11 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,940,850 to Harish, et al (hereinafter, "Harish"). Appellants traverse these rejections. In the interest of brevity, arguments set forth in the Appeal Brief will not be repeated in this document. Nonetheless, these arguments are incorporated herein.

A. Legal Standard for Anticipation

The standard for lack of novelty, that is, for "anticipation," under 35 U.S.C. §102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 231 USPQ 81, 90 (Fed. Cir. 1986). Invalidity for anticipation requires that all of the elements and limitations of the claims be found within a single prior art reference. *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991). Every element of the claimed invention must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (finding that the jury had been erroneously instructed that anticipation may be shown by equivalents, a legal theory that is pertinent to obviousness under Section 103, not to anticipation under Section 102). "The identical invention must be shown in as complete detail as is contained in the patent claim." MPEP §2131 (7th Ed. 1998) (citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). Furthermore, functional language, preambles, and language in "whereby," "thereby," and "adapted to" clauses cannot be disregarded. *Pac-Tec, Inc. v. Amerace Corp.*, 14 USPQ2d 1871 (Fed. Cir. 1990).

"It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office." *Ex parte Skinner*, 2 USPQ2d 1788, 1788-1789 (Bd. Pat. Int. 1986) (holding that examiner failed to establish *prima facie* case of anticipation). The examiner has "the burden of proof . . . to produce the factual basis for its rejection of an application under sections 102 or 103." *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) (quoting *In re Warner*, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)). Only if that burden is met, does the burden of going forward shift to the applicant.

B. Claim 1

Claim 1 stands rejected for anticipation under 35 U.S.C. §102. This rejection is traversed based on the arguments presented in the Appeal Brief, which are incorporated herein, and on the following arguments.

Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Claim 1 recites limitations that are neither disclosed nor suggested by Harish. Therefore Harish cannot anticipate claim 1.

1. Harish Neither Discloses nor Suggests an Arrangement that Includes First and Second Tables

Independent claim 1 includes limitations directed to "an agent coupled to a host, the agent having volatile memory for storing a *first table*, the table having entries to map the virtual storage segments to the storage locations; and a controller coupled to the agent, the controller having non-volatile memory for storing a *second table* . . . " The Examiner's Answer maintains the position that Harish discloses these limitations, and cites the Abstract

and column 2, lines 25-34, and column 4, lines 37-50 to support the rejection.

Appellants disagree. The text of the Abstract and column 2, lines 24-34 are excerpted in the Appeal Brief filed November 3, 2006, and need not be repeated herein. The text of colum 4, lines 37-50 reads as follows:

> The system described herein intercepts the write-access fault and tests whether the physical address references dynamic data in ROM at step 308. If not, the write attempts was an error indicating a static data page and an error exception is raised at step 310, whereupon the process ends at step 311. If the physical address is in ROM, the system of the present invention creates a page in RAM and copies the ROM page to the RAM page at step 312. The page table entry 203 (FIG. 2) is modified so that the physical address 206 references the RAM page 218. This is shown at step 314 wherein the page table entry 314 is replaced with an entry mapped to RAM. The new physical reference is used to write the modified data at step 316.

Nothing in the cited text discloses (or even suggests) an agent coupled to a host, the agent having volatile memory for storing a *first table*, the table having entries to map the virtual storage segments to the storage locations; and a controller coupled to the agent, the controller having non-volatile memory for storing a *second table*, as recited in claim 1. For this reason alone, the Examiner's Action fails to establish a *prima facie* case of anticipation.

The Examiner's Answer further asserts that "page table entries in both RAM and ROM contain a mapping of virtual address to physical address." Initially, Appellants note that this assertion does not appear to correspond to the claim language. Further, Appellants note that the Examiner's Answer provides *no evidence of record whatsoever* to support this assertion. Still further, Appellants note that this assertion is factually incorrect. Contrary to the Examiner's assertion, Harish discloses an arrangement which uses only a *single* page table, identified as page table 202. The page table entries 203 in the table 202 may point either to data stored in RAM or data stored in ROM, however the page table entries 203 all reside within a *single* table 202; the entries 203 do <u>not</u> exist in both RAM and ROM.

<u>2. Harish Neither Discloses nor Suggests an Arrangement in which the Contents of a First Table are Replaced by the Content of a Second Table</u>

Independent claim 1 further includes a limitation reciting that "the controller intermittently causing *contents of the first table* to be replaced by *contents of the second table* . . ." The Examiner's Answer maintains the position that Harish discloses these limitations, and cites the Abstract and column 2, lines 10-19, and column 4, lines 43-50 to support the rejection.

Appellants disagree. Initially, Appellants note that in view of the fact that Harish fails to disclose a first table and a second table, as set forth above, it is logically impossible for Harish to disclose replacing the contents of a first table with the contents of a second table. Further, the text of the column 2, lines 24-34 is excerpted in the Appeal Brief filed November 3, 2006, and the text of column 4, lines 43-50 is excerpted above, and need not be repeated here. Nothing in the cited text discloses (or even suggests) the controller intermittently causing *contents of the first table* to be replaced by *contents of the second table*, as recited in claim 1.

The Examiner's Answer further asserts that "the ROM data is loaded into RAM when memory is modified." Initially, Appellants note that this assertion does not appear to correspond to the claim language. Further, Appellants note that the Examiner's interpretation of the teaching of Harish is clearly factually incorrect. Contrary to the Examiner's assertion, the data stored in ROM and RAM in Harish are *not* table entries. Rather, the data is raw data to which the table entries 203 point.

In sum, Harish fails to disclose or to suggest both structural and functional elements recited in claim 1. Therefore, the rejection of claim 1 under 35 U.S.C. 102(b) is improper and must be overturned.

C. Claim 2

Independent claim 2 recites limitations including "wherein the second table identifies an

alternate storage location within the storage locations." The Final Action asserted that Harish discloses this limitation, and cited the Abstract and column 2, lines 10-51 to support the rejection. Appellants disagree. The Examiner's Answer maintains the assertion, and now cites column 3, lines 57-65 and column 4, lines 6-20 to support the rejection.

Initially, Appellants note that in view of the fact that Harish fails to disclose a first table and a second table, as set forth above, it is logically impossible for Harish to disclose an arrangement wherein the *second* table identifies an alternate storage location within the storage locations.

Further, Appellants disagree. The cited text reads as follows:

> Virtual memory management systems separate the logical system memory reference from the physical address of the referenced object. This allows the system to reference a greater amount of memory than is physically present in a system. Virtual memory management schemes typically are based on pages of memory. At any point in time a number of pages are present in memory. These pages are tracked using a page table that cross references the virtual address to the location of the actual page containing the memory data. If an address reference is requested that does not exist in the page table, a page fault occurs requiring the referenced page to be loaded into memory. Memory pages are typically managed on a least recently used basis. The system will discard the least recently used page in memory and replace it with the one requested. If necessary, the page to be discarded is written out to storage before the page is freed.
>
> The translation of a virtual address to the physical address is performed using a page table with a page table entry for each page in memory. FIG. 2 illustrates such a table 202. The page table entry 203 for a page containing dynamic data includes a virtual address 204 and a physical address 206. A page table can reference physical addresses in ROM 210 or RAM 216. In the preferred embodiment, the page table entry for a page containing ROM dynamic data is created with the physical address 206 pointing 208 to the ROM data page 212 containing the data. The protection for page table entry 203 is set to "read-only" even though it references dynamic data. This protection setting will cause the operating system to raise a "write-access" exception if an attempt is made to write to the data area.

Nothing in this text discloses (or even suggests) an arrangement wherein the second table identifies an alternate storage location within the storage locations, as recited in claim 2. Therefore, Harish cannot anticipate claim 2.

The Examiners Answer appears to address claim 2 on page 8 in response to what the Examiner's Answer characterizes as "Argument B." Without judging the technical accuracy or legal merits of the assertions made in this section, they appear to be entirely unrelated to the language of claim 2.

D. Claim 3

The Examiner's Answer maintains the rejection of claim 3 based on a subset of the text cited in the final Action. No new arguments are presented in the Examiner's Action. Therefore, Applicant's reassert the arguments submitted in the Appeal Brief.

E. Claim 4

Claim 4 recites limitations including "an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments." The final Action asserted that Harish discloses this limitation, and cited the Abstract and column 2, lines 10-51 to support the rejection. The Examiner's Answer maintains the rejection, and now cites column 3, line 57 to column 4, line 5 to support the rejection.

Appellants disagree. The cited text reads as follows:

> Virtual memory management systems separate the logical system memory reference from the physical address of the referenced object. This allows the system to reference a greater amount of memory than is physically present in a system. Virtual memory management schemes typically are based on pages of memory. At any point in time a number of pages are present in memory. These pages are tracked using a page table that cross references the virtual address to the location of the actual page containing the memory data. If an address reference is requested that does not exist in the page table, a page fault occurs requiring the referenced page to be loaded into memory. Memory pages are typically managed on a least recently used basis. The system will discard the least recently used page in memory and replace it with the one requested. If necessary, the page to be discarded is written out to storage before the page is freed.

Nothing in this text discloses (or even suggests) an arrangement comprising an alternate

storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments, as recited in claim 4. Therefore, Harish cannot anticipate claim 4.

F. Claim 5

Claim 5 recites limitations including "an I/O operation accesses information on both the storage location and the alternative storage location." The final Action asserted that Harish discloses this limitation, and cited the Abstract and column 2, lines 10-51 to support the rejection. The Examiner's Answer maintains the rejection, and now cites column 4, lines 6-20 to support the rejection.

Appellants disagree. The cited text reads as follows:

> The translation of a virtual address to the physical address is performed using a page table with a page table entry for each page in memory. FIG. 2 illustrates such a table 202. The page table entry 203 for a page containing dynamic data includes a virtual address 204 and a physical address 206. A page table can reference physical addresses in ROM 210 or RAM 216. In the preferred embodiment, the page table entry for a page containing ROM dynamic data is created with the physical address 206 pointing 208 to the ROM data page 212 containing the data. The protection for page table entry 203 is set to "read-only" even though it references dynamic data. This protection setting will cause the operating system to raise a "write-access" exception if an attempt is made to write to the data area.

Nothing in this text discloses (or even suggests) an arrangement wherein an I/O operation accesses information on both the storage location and the alternative storage location., as recited in claim 5. Therefore, Harish cannot anticipate claim 5.

G. Claim 6

Claim 6 recites limitations including "wherein a bitmap designates blocks at the alternative storage location to use for the I/O operation." The final Action asserted that Harish discloses this limitation, and cited the Abstract and column 2, lines 10-51 to support the rejection. The Examiner's Answer maintains the rejection, and now cites column 3, line 57 to column 4, line 5 to support the rejection.

Appellants disagree. The cited text reads as follows:

> Virtual memory management systems separate the logical system memory reference from the physical address of the referenced object. This allows the system to reference a greater amount of memory than is physically present in a system. Virtual memory management schemes typically are based on pages of memory. At any point in time a number of pages are present in memory. These pages are tracked using a page table that cross references the virtual address to the location of the actual page containing the memory data. If an address reference is requested that does not exist in the page table, a page fault occurs requiring the referenced page to be loaded into memory. Memory pages are typically managed on a least recently used basis. The system will discard the least recently used page in memory and replace it with the one requested. If necessary, the page to be discarded is written out to storage before the page is freed.

Nothing in this text discloses (or even suggests) an arrangement wherein a bitmap designates blocks at the alternative storage location to use for the I/O operation, as recited in claim 6. Therefore, Harish cannot anticipate claim 6.

H. Claim 7

The Examiner's Answer fails to establish a *prima facie* case that Harish anticipates independent claim 7. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 7 recites:

> 7. A system for mapping a virtual disk segment to a storage location within a storage device, such that a host queries said system to determine said storage location for input/output operations, said system comprising:
>
> a first table having a first table entry mapping the virtual disk segment to the storage location;
>
> a second table having a second table entry corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location;
>
> a plurality of variables indicating states of an entry in the first table or the second table;
>
> an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier;
>
> a first memory to store the first table; and
>
> a second memory to store the second table.

Neither the final Action nor the Examiner's Answer provide any citation to relevant portions of Harish to support the assertion that Harish discloses limitations of claim 7, instead merely asserting that "[claim] 7 is essentially the system claim for claim 1." The Action sets forth no evidence or argument that Harish discloses (or even suggests) structural elements corresponding to a first table having a first table entry mapping the virtual disk segment to the storage location, and a second table having a second table entry corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location, as recited in claim 7. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 7 because Harish

neither discloses (nor even suggests) limitations recited in independent claim 7. Claim 7 recites "a plurality of variables indicating states of an entry in the first table or the second table, and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier" The Action asserts that Harish discloses this limitation, and cites Fig. 3, column 4, lines 20-37; column 2, lines 19-51 and column 3, lines 56 to column 4, line 5 to support the rejection. Applicant disagrees. The cited text reads as follows:

> ROM data is loaded into random access memory (RAM) only when that data is actually being modified. An attempt is detected to write to dynamic data in ROM and generates a write-access fault. The write-access fault is captured causing the system to copy the ROM data to RAM, change a page table entry to point to the RAM copy, and then write the data. This mechanism avoids loading ROM data that is not modified thereby reducing the RAM requirements for a given system.
>
> Virtual memory management systems separate the logical system memory reference from the physical address of the referenced object. This allows the system to reference a greater amount of memory than is physically present in a system. Virtual memory management schemes typically are based on pages of memory. At any point in time a number of pages are present in memory. These pages are tracked using a page table that cross references the virtual address to the location of the actual page containing the memory data. If an address reference is requested that does not exist in the page table, a page fault occurs requiring the referenced page to be loaded into memory. Memory pages are typically managed on a least recently used basis. The system will discard the least recently used page in memory and replace it with the one requested. If necessary, the page to be discarded is written out to storage before the page is freed.

Nothing in this text discloses (or even suggests) a plurality of variables indicating states of an entry in the first table or the second table, and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier, as recited in claim 7. To the contrary, Harish fails even to mention a logical unit, a logical unit number identifier, or a block identifier.

In sum, the Action fails to establish a *prima facie* case of anticipation. Furthermore, Harish fails to disclose or suggest elements of claim 7, and therefore cannot anticipate

independent claim 7.

II. Rejections Under 35 U.S.C. §103

Claims 12-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Harish in view of U.S. Patent No. 5,483,649 to Kuznetzov (hereinafter, "Kuznetzov"). The Examiner's Answer sets forth no new assertions regarding these claim rejections. Therefore, in the interest of brevity, arguments set forth in the Appeal Brief will not be repeated in this document. Nonetheless, these arguments are incorporated herein.

CONCLUSIONS

The Examiner's Answer fails to provide an evidentiary record sufficient to support an anticipation rejection of claims 1-11 under 35 U.S.C. §102. Therefore, Appellants urge the Board to reverse the examiner's rejections under 35 U.S.C. §102 of claims 1-11.

Further, Harish, alone or in combination with Kuznetzov, fails to disclose or suggest limitations recited in pending claims 12-16. Therefore, Harish, alone or in combination with Kuznetzov, cannot be used to establish the required prima facie case of obviousness under 35 U.S.C. §103. Therefore, Appellants urge the Board to reverse the examiner's rejections under 35 U.S.C. §103 of claims 12-16.

Respectfully submitted,

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Date: March 12, 2007